DESIGN OF CONVOLUTIONAL ENCODER USING 16 BIT REVERSIBLE LOGIC VEDIC MULTIPLIER

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ABSTRACT

This paper is focuses the recognition of capable of logic design of crypto system, the convolution encoder which leads to faster speed and improve delay the convolutional encoder the design are basically encoders be very important for particularly low probability error used at high data rate the system is used to realized using simulation and synthesized using modelsim6.3f and cadence for RTL Design

Keywords- Convolutional Encoder, reversible logic, power dissipation, Verilog HDL

INTRODUCTION

An encoder is a device that converts in order one format of code to a new format of code, it is for the purposes of faithful of improvement of a message bits, the convolutional encoder is error correction scheme the encoder terms is used for the process of analog-to-digital convertor an encoder is a device, transducer, circuit, software program or person that converts the information from one format of code to another format of code it is used for the purpose secrecy, speed, standardization compress or security, this code is often deep space communication and it is used more in recently in digital wireless communication in more real time application in video and audio application ,the cost of the convolutional encoder codes are used for error modification the cost of convolutional encoder is expansive for specification design because of the patent issue , to realization of adaptive convolutional encoder on FPGA on board is very demanding

We concern with the design and implementation of a convolutional encoder it is the necessary block in digital communication systems using the FPGA technology

The convolutional codes offers alternative block code for transmission over the noise channel convolution coded can be applicable to a permanent input stream and block of data A simple convolutional encoder is as shown in the "fig 1" ,

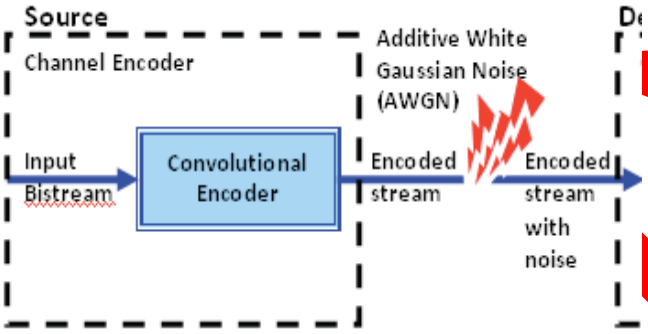


Figure1:Convolutional encoder

Above block diagram shows the basic convolutional encoder in the source terminal channel encoder is used input bistreams to the convolutional encoder the output of the encoded stream with additive white noise and finally encoded stream with noise

A. convolution Encoder design using 16 bit reversible logic Vedic multiplier

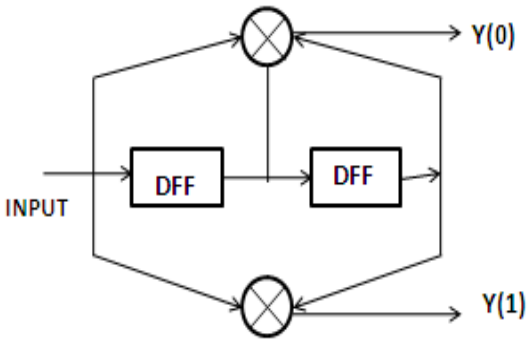
Convolutional codes is used to keep in order by adding redundant bits to a binary data, the convolutional encoder compute each n-bit symbol of output sequence from the linear operation of the current input of k-bit symbol the constant shift register the rate K n convolutional encoder it is a process k-bit input symbol and it compute the n-bit output symbol with the every shift shift register update the commonly specified convolutional codes of three parameters they are

n= is the no of output bits
k= is the no of input bits
m=is the no of memory registers

The amount k/n is consider as code rate, it is measured in terms of efficiency of code. Normally parameter range of k and n is from 1 to 8, the code rate as low or even long that have been employed
The quantity of constant length L of the code is defined as
Constant Length, L = k (m-1)
The constant length represent the number of memory bits in the encoder that memory bits effects the general n output bits
And the constant length it is also referred as capital letter K, it is also confused as lower case
Convolutional coding been used in communication system together with in wireless communication and deep space communication, the convolutional coding is used continues input stream can be applied using

block of data, it contains one or more DFF and multiple XOR gates are associated to sum stages of current input to produce output is polynomial

A convolutional encoder is mainly a machine, where the output is the function of current state and the current input, it consists of one or more XOR gate and shift register



Figure,2: Convolutional encoder of rate ½ using 16bit reversible logics

The above "fig 2", shows the 16 bits of encoder information for a single bit of input information, so it is called as the rate of ½ encoder

The reversible logic circuits is a method of one circuit I is the recovery of energy level it employs the concept of reversible logic the circuits is computes if it is reversible there the input and output is the one to one mapping between them, so that output of the circuit is able to determine input of the circuits The "fig 3", shows the block diagram of convolution encoder design using Vedic multiplier

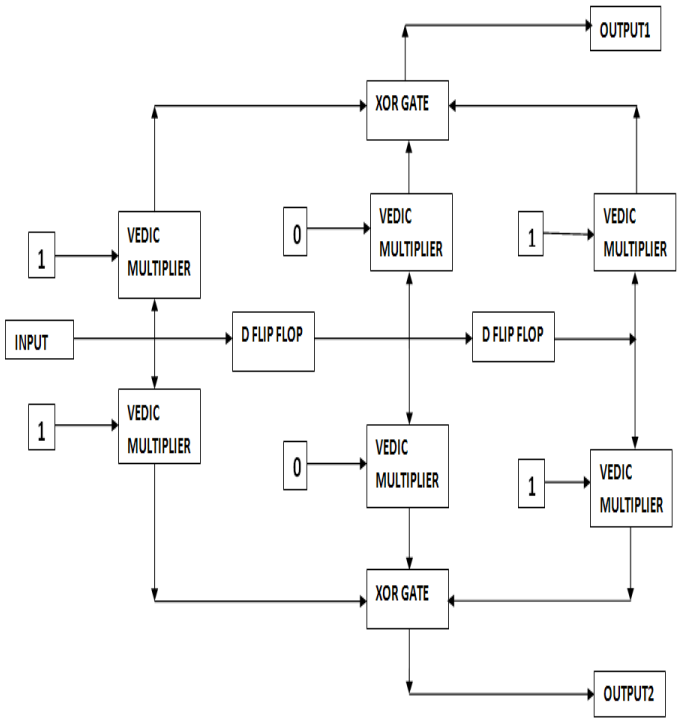


Figure 3: convolutional encoder using Vedic multiplier

B. OPERATION OF REVERSIBLE LOGIC

The signal power improving to the prefers extent is very potential with asymptotically adiabatic reason, anywhere the power is transfer within a circuit avoid any sudden release high possible to ground base on current experience, scheming such circuit involve in the logical operation utilize include to be reversible logic is used in environment and CMOS skill does not get better signal power it is leads to significant power waste and high temperature dissipation

The reasonable reversible is relate to the materials is reversibility of the structure the system has sum reflect a few degree of the calculation is performed a bits removable in space of heat has an expected power cost of regarding 0.003aJ which is typically power is dissipate as power into the situation as a part of indication of power cannot be adiabatically improved except slot in reasonable to the circuit is used in the conventional circuit bit removable of power irrelevant of comparison to other losses , the other magnitude of advanced power per switch event the raising technology like cellular automation they can made simple as preferred by switching id more gradually slowly is unchanged by the speed so it is essential to design system utilize for logical or clock signal in adding to archive some degree of logical reversibility and the circuit design view point of reversible logic and adiabatic process are attractive but they earn a range of cost, it as ensure-aware the circuit is used to involve tradeoff among of them circuit area, performance time, and power it complementary that effects of the erasures and adiabatic operation

C. DESIGN CONSTRAINTS OF REVERSIBLE LOGICS

The following are the significant design constraints of reversible logics are

- The reversible logics does not permit fan-outs
- The reversible logics circuits be supposed to have small amount quantum cost
- The design can be optimize to create small amount of garbage outputs
- Reversible logics must used min no of constant inputs
- Reversible logics must be used min logical depth

In the conventional logical circuit combination, single usually start with a universal gate records and sum plans of a Boolean purpose, the main aim to find logical circuit equipment of the Boolean purpose and min of a given cost The no of gates in the circuits' mixture is just a special case in fan out permitted for all gates must be reversible

The reversible logics circuits are supposed to have sum features

- The use min no of reversible gates
- The use min no of garbage outputs
- The use min constant inputs

The output is not used for additional computation of reversible logic is called garbage output and the quantum processor consisting quantum logical gates and quantum logical gate execute simple united process is on

A quantum computer consists of single or more than two states system is called as qubits and it represents the simple Unit of information matching to their bits values zero or one and with smallness of its two face issue they are

- The large quantity of power is get dissipated in VLSI circuits
- The amount of a transistor are future the quantum limit this phenomena is get approach

The min no of the reversible logic gates, quantum cost and garbage output is to focus to study in reversible logical syntheses

D. VEDIC MULTIPLIER FOR 16X16 BITS USING REVERSIBLE LOGIC

The architecture of 16X16 Vedic multiplier reversible logic using Urdhva Tiryagbhyam sutra is as shown in "fig 4" ,the multiplication architecture is using implementation of four 8X8 Vedic multiplier using two 16 bit binary adder stage, then the output is given as

$X \times Y = (Z31 - Z16)$ & $(Z15 - Z8)$ & $(Z7 - Z0)$

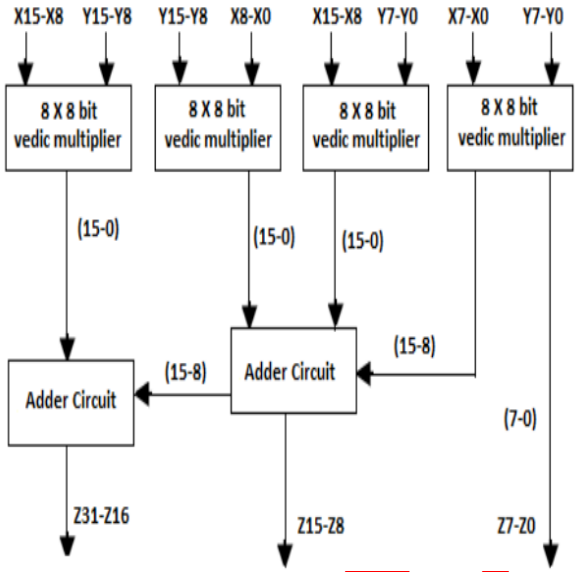


Figure 4: Hardware Realization of 16x16 Bit Multiplication reversible logic using Urdhava Tirya Kbhyam Sutra

The Vedic Multiplier for 16x16 Bits using reversible logic as speed is always multiplication operation, it is used to increase the speed it is used to reducing in computation process the efficiency and speed of the multiplier is used to determined the three main constraint and performance of the system is power, area and speed requirement, Vedic mathematics is Mainly based on world-formula or six principles are in terms of sutra, the integrating multiplication using Vedic mathematical techniques and saving the results in computational time , thus the integrating Vedic mathematics using multiplier design will be get enhanced the operation multiplication speed there is a reduction in time of computation an increasing the speed of multiplier

E.EXPERIMENTAL RESULTS AND DISCUSSIONS

1) RTL Schematics view

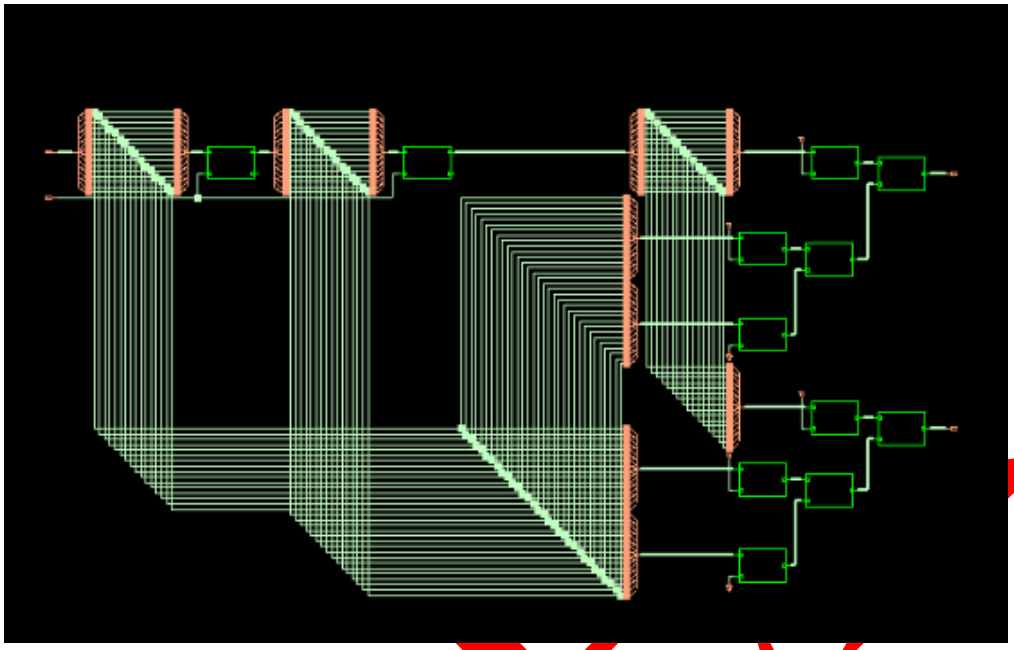


Figure 5: RTL Schematic of Convolutional Encoder using 16 Bit reversible logic Vedic multiplier

2). Vedic multiplier

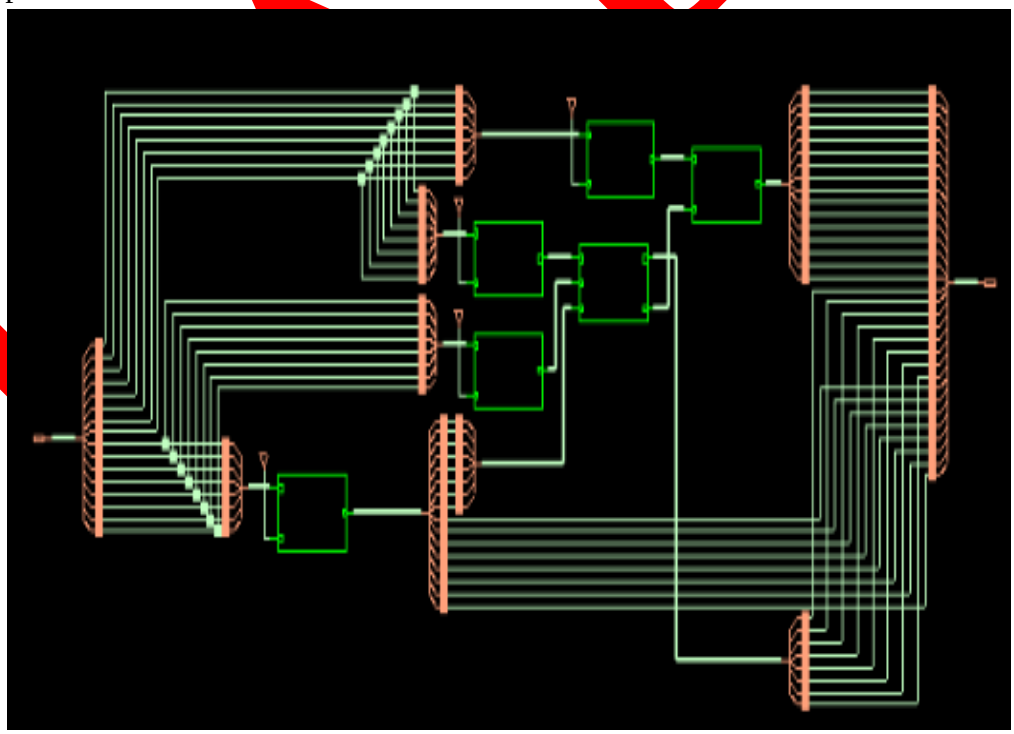


Figure 6: convolution encoder using Vedic multiplier

3). Adder using Vedic multiplier

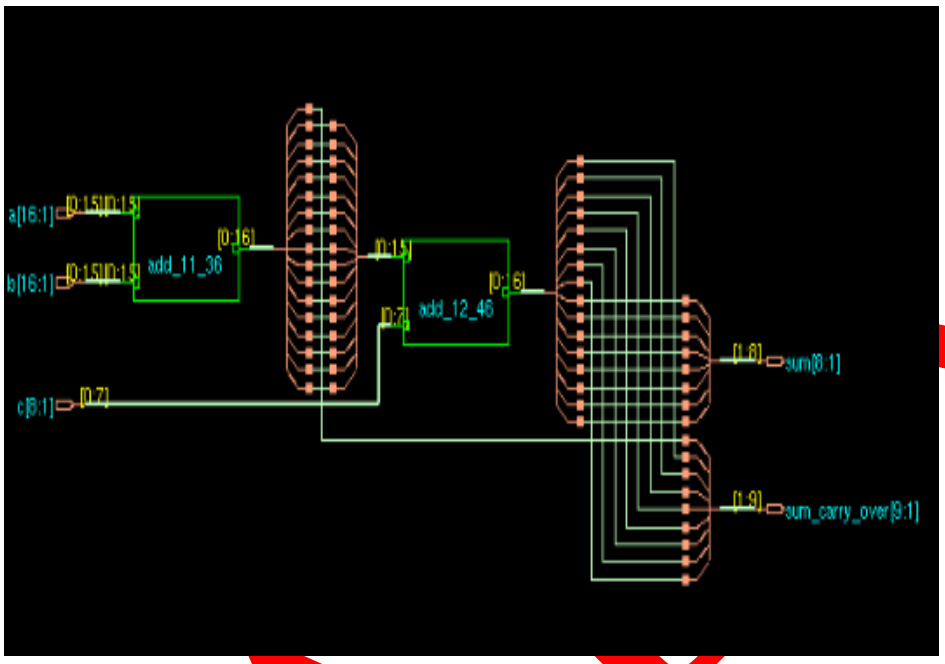


Figure 7: Adder using multiplier

4). Adder multiplier

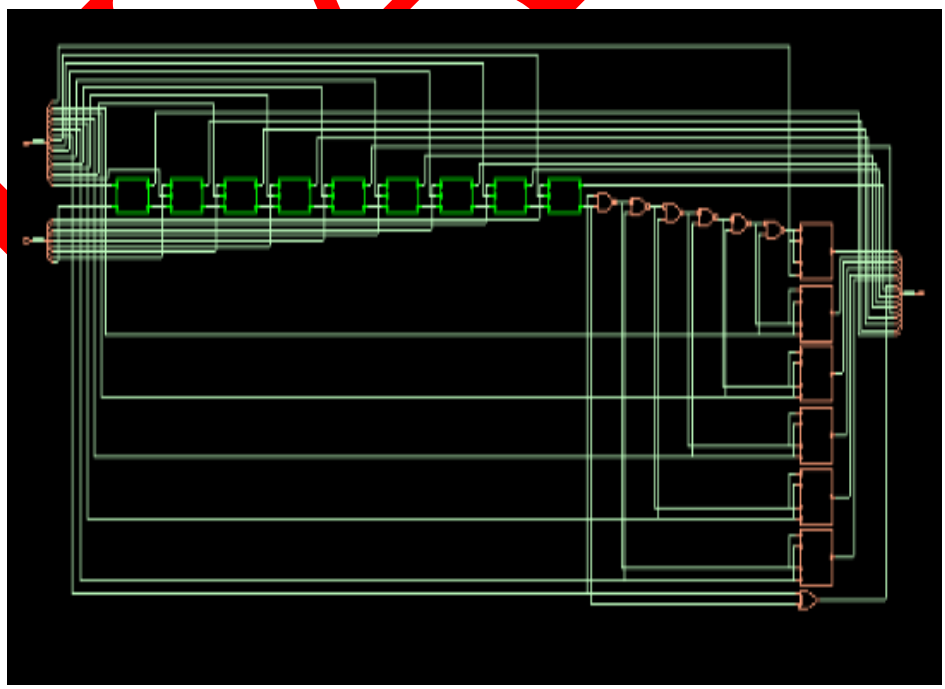


Figure 8: Adder using Vedic multiplier

5). Vedic multiplier

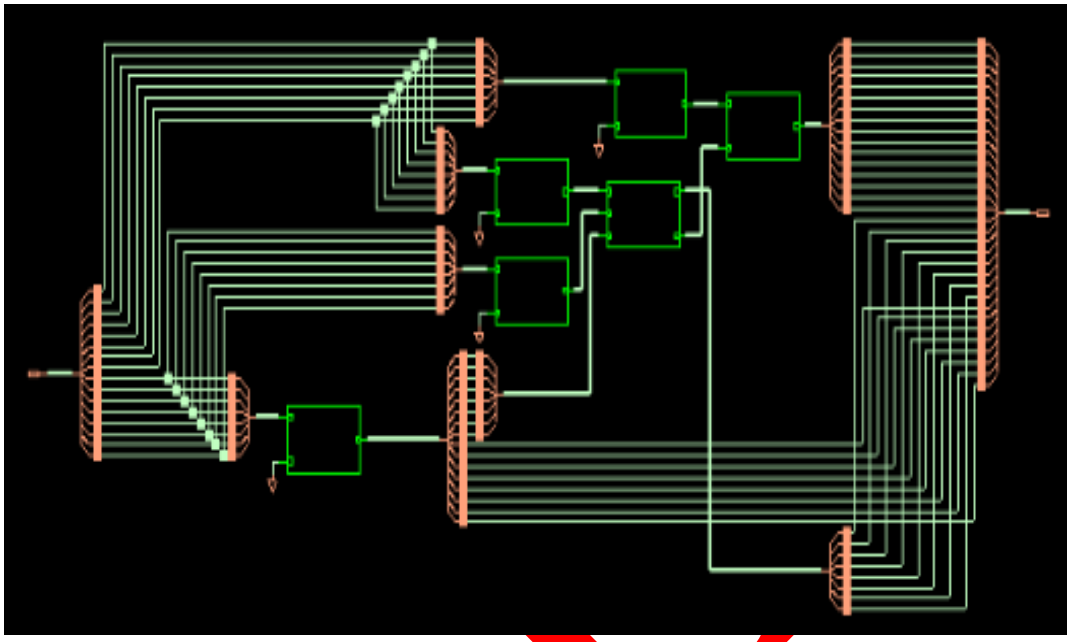


Figure 9: convolution encoder using Vedic multiplier

6). XOR 32bits

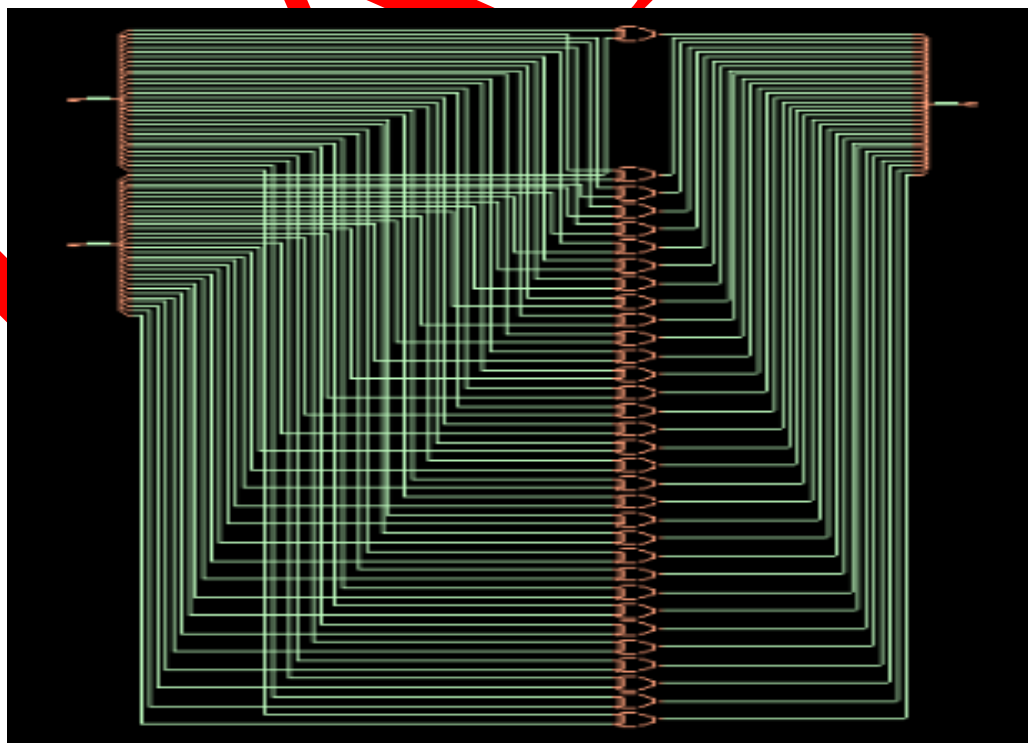


Figure 10: XOR 32bits

7).Simulation Results

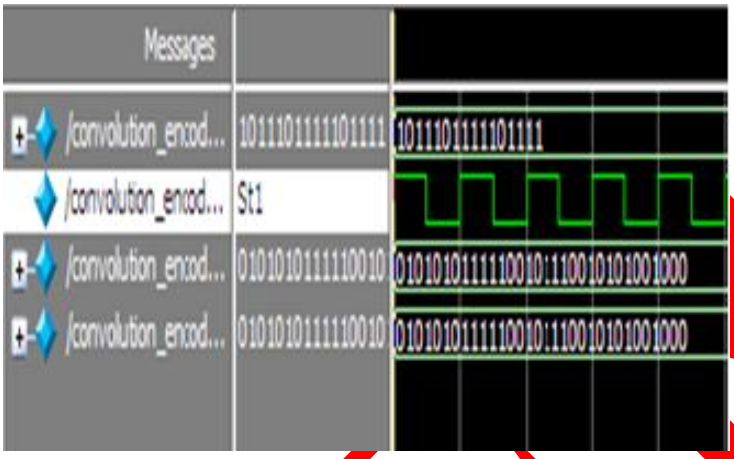


Figure 11: Simulation Results of Convolutional Encoder Using 16 Bit reversible logic using Vedic multiplier

Table No. 1: Synthesis Results

Convolutional encoder design using 16bit reversible logics Vedic multiplier	***Leakage power(nw)***	***Dynamic power(nw)***	***Total power(nw)***
	138602.162	1201314.845	1339917.008

CONCLUSION

This paper is works to implement design and synthesis of convolutional encoder using 16bit reversible logic Vedic multiplier the convolution code is used to encode using cadence tool very important for low error probability high data rate synthesis using cadence and simulation using modelsim6.3f for a given design

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